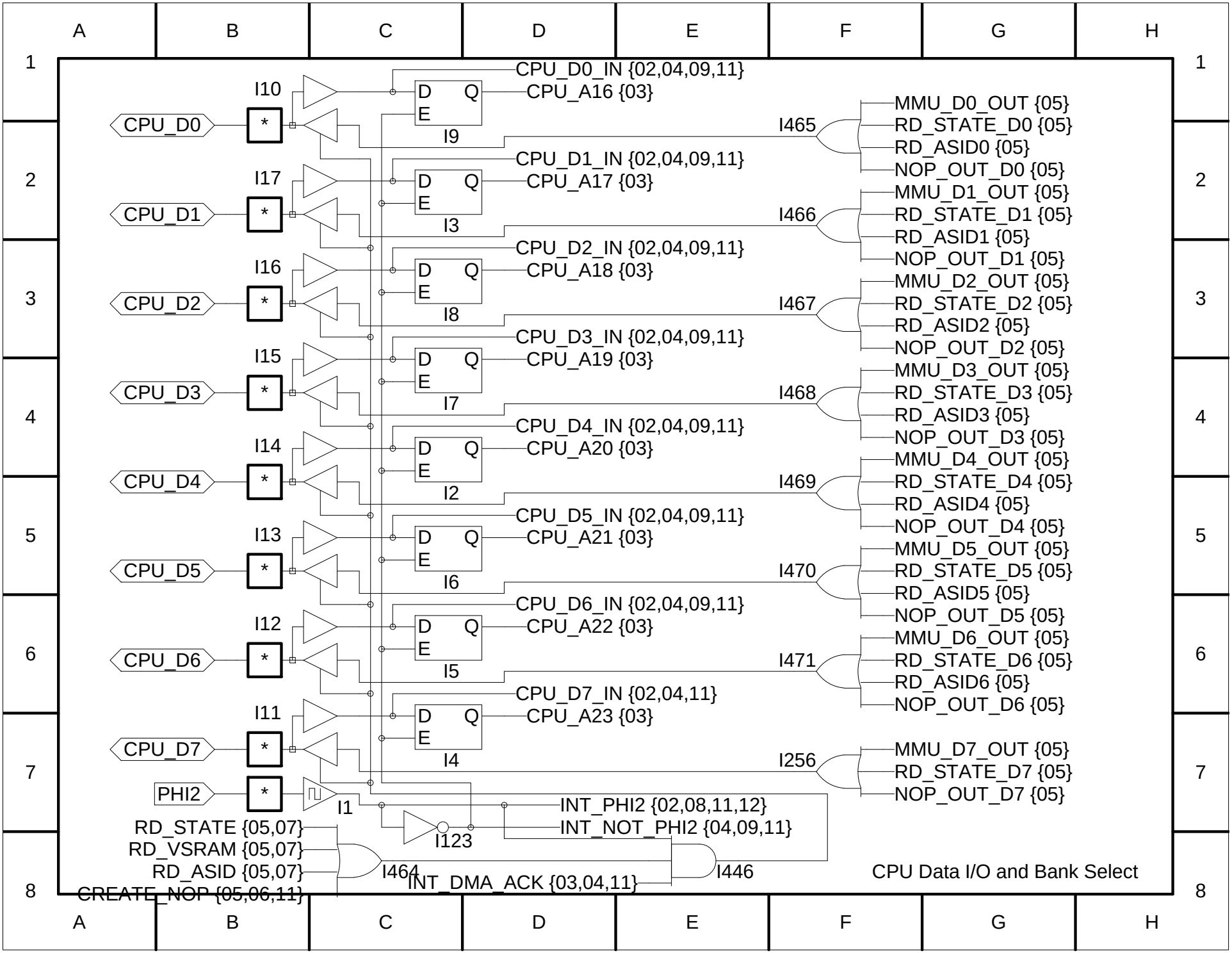
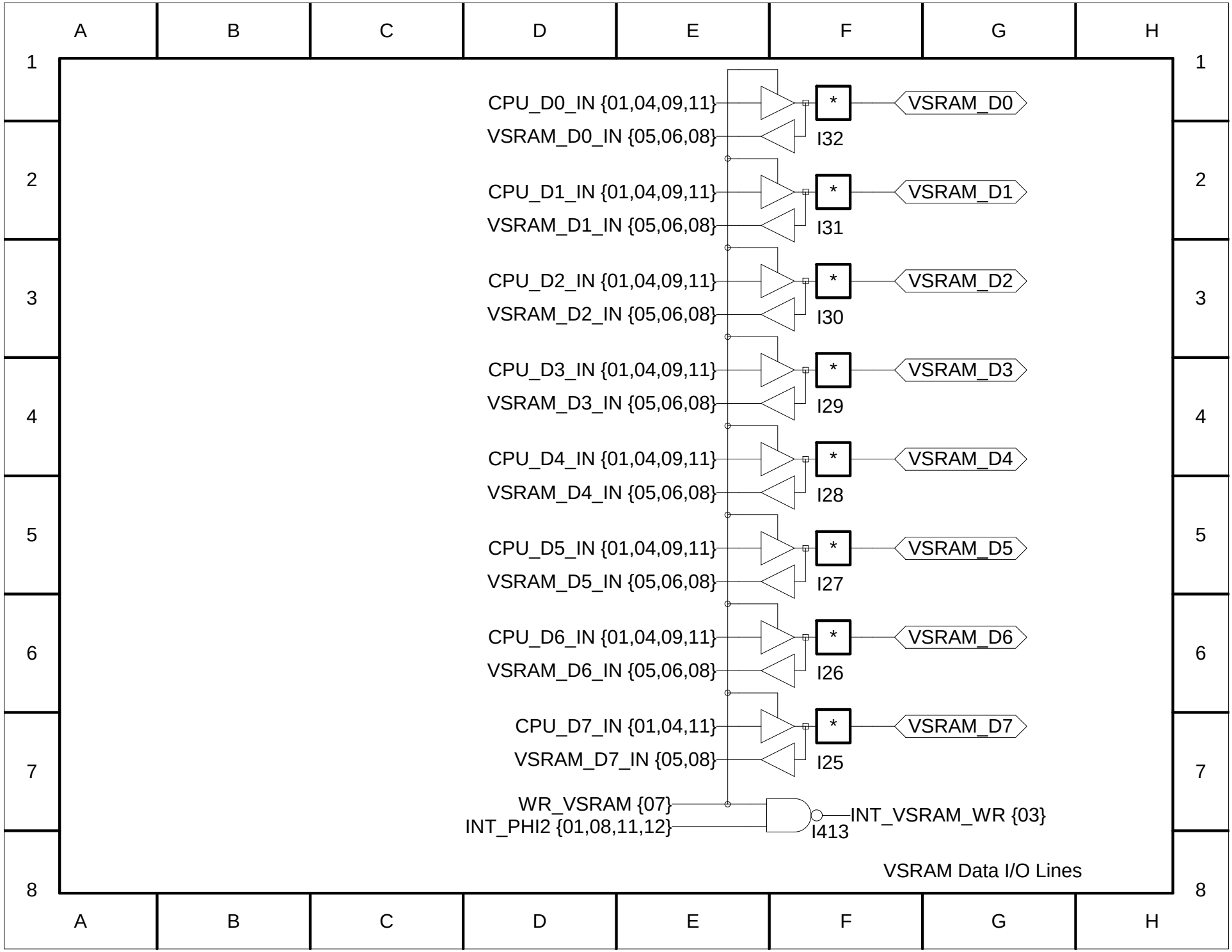
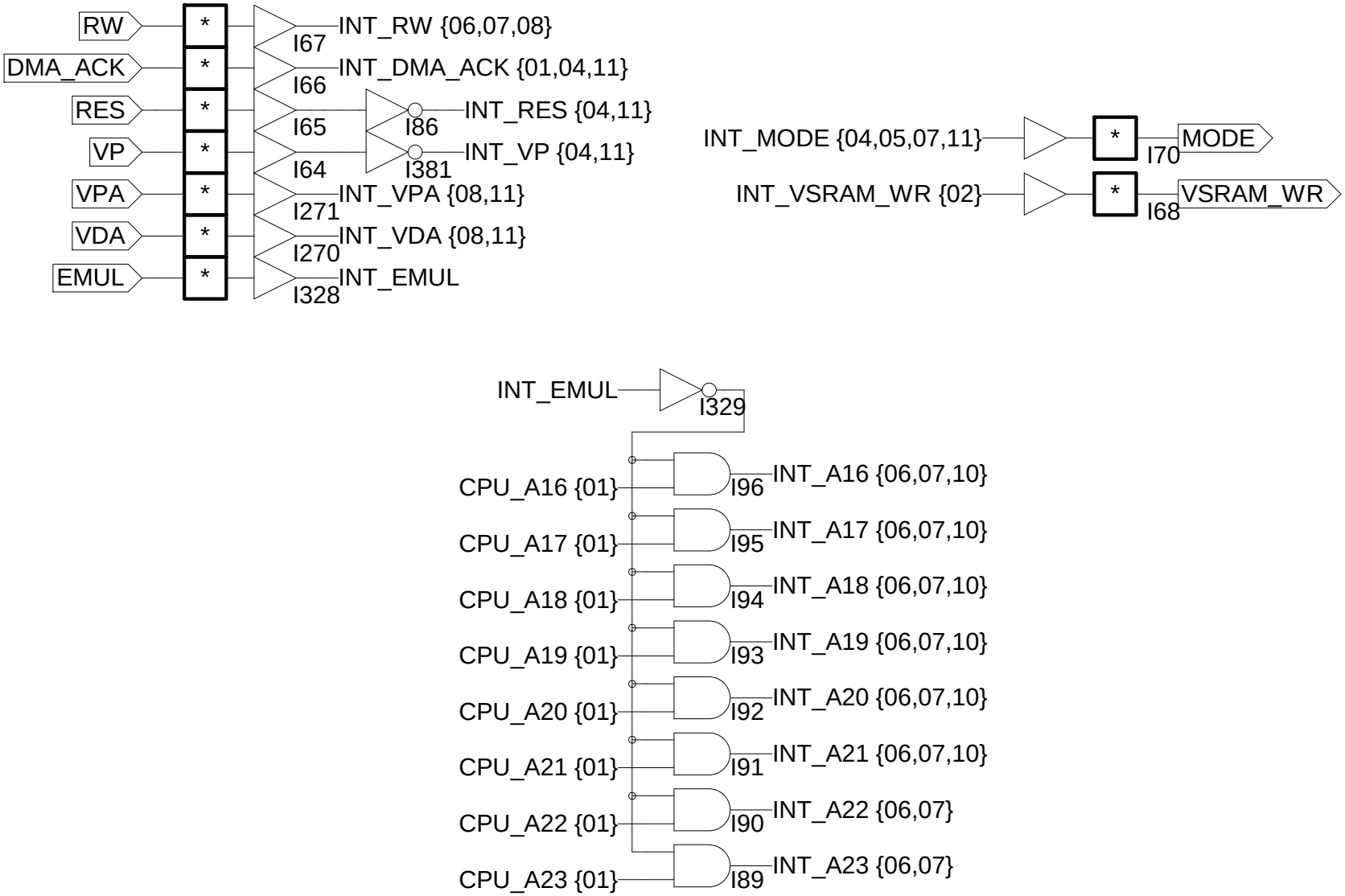
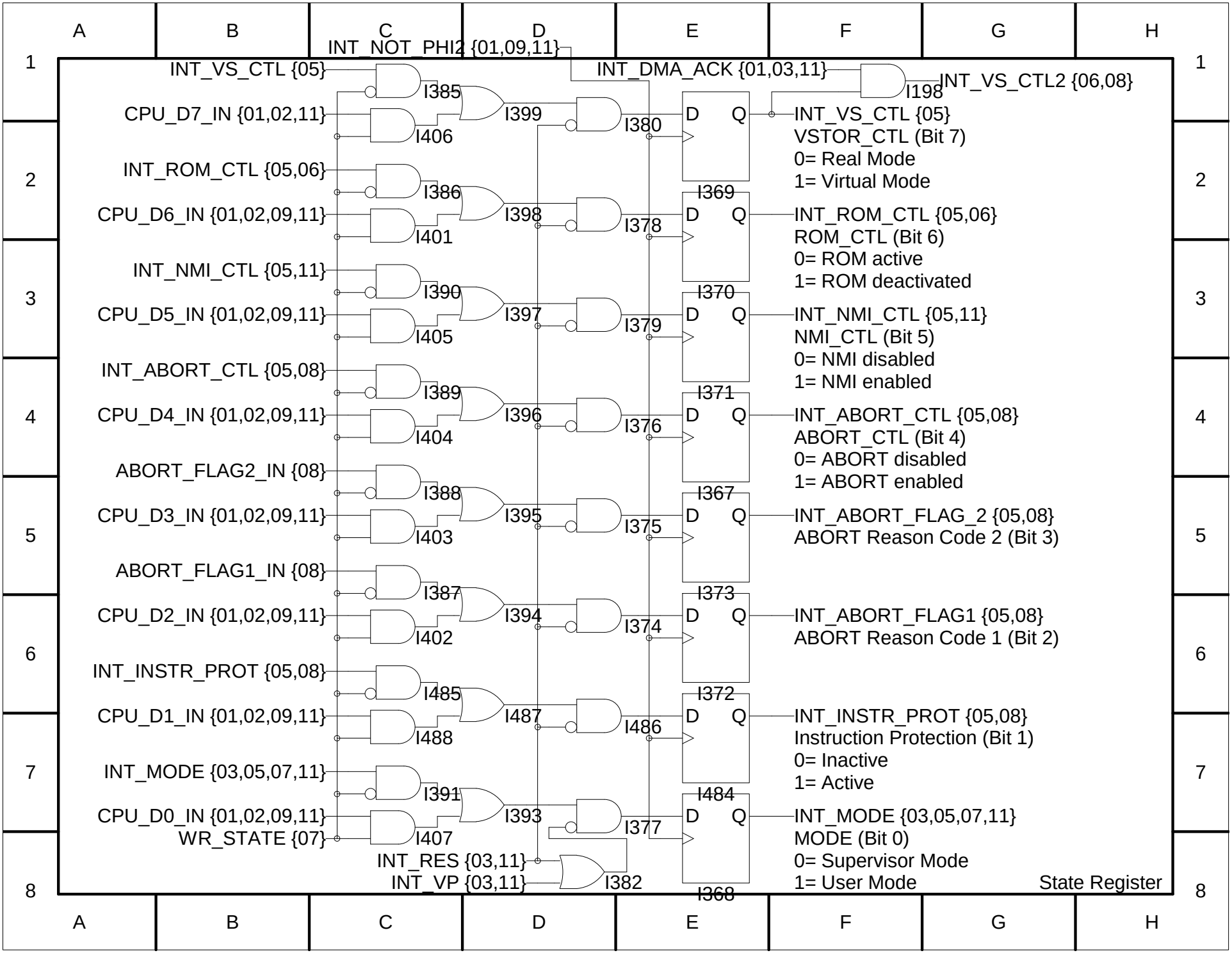
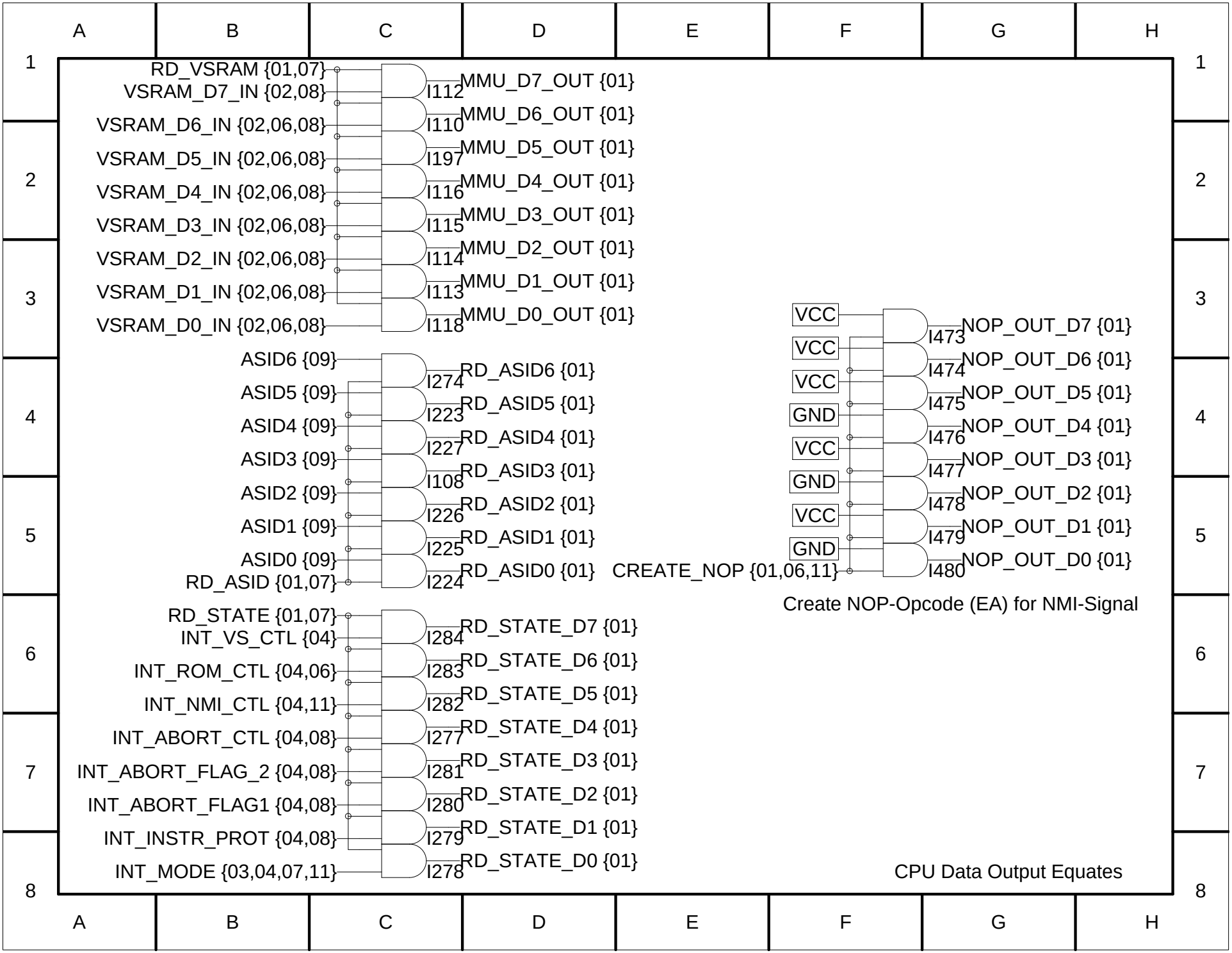

CPU_D0
CPU_D1
CPU_D2
CPU_D3
CPU_D4
CPU_D5
CPU_D6
CPU_D7
PHI2
I10
I17
I16
I15
I14
I13
I12
I11
I1
I9
I3
I8
I7
I2
I6
I5
I4
I123
I465
I466
I467
I468
I469
I470
I471
I256
I464
I446
CPU_D0_IN {02,04,09,11}
CPU_A16 {03}
CPU_D1_IN {02,04,09,11}
CPU_A17 {03}
CPU_D2_IN {02,04,09,11}
CPU_A18 {03}
CPU_D3_IN {02,04,09,11}
CPU_A19 {03}
CPU_D4_IN {02,04,09,11}
CPU_A20 {03}
CPU_D5_IN {02,04,09,11}
CPU_A21 {03}
CPU_D6_IN {02,04,09,11}
CPU_A22 {03}
CPU_D7_IN {02,04,11}
CPU_A23 {03}
MMU_D0_OUT {05}
RD_STATE_D0 {05}
RD_ASID0 {05}
NOP_OUT_D0 {05}
MMU_D1_OUT {05}
RD_STATE_D1 {05}
RD_ASID1 {05}
NOP_OUT_D1 {05}
MMU_D2_OUT {05}
RD_STATE_D2 {05}
RD_ASID2 {05}
NOP_OUT_D2 {05}
MMU_D3_OUT {05}
RD_STATE_D3 {05}
RD_ASID3 {05}
NOP_OUT_D3 {05}
MMU_D4_OUT {05}
RD_STATE_D4 {05}
RD_ASID4 {05}
NOP_OUT_D4 {05}
MMU_D5_OUT {05}
RD_STATE_D5 {05}
RD_ASID5 {05}
NOP_OUT_D5 {05}
MMU_D6_OUT {05}
RD_STATE_D6 {05}
RD_ASID6 {05}
NOP_OUT_D6 {05}
MMU_D7_OUT {05}
RD_STATE_D7 {05}
NOP_OUT_D7 {05}
INT_PHI2 {02,08,11,12}
INT_NOT_PHI2 {04,09,11}
RD_STATE {05,07}
RD_VSRAM {05,07}
RD_ASID {05,07}
CREATE_NOP {05,06,11}
INT_DMA_ACK {03,04,11}
CPU Data I/O and Bank Select

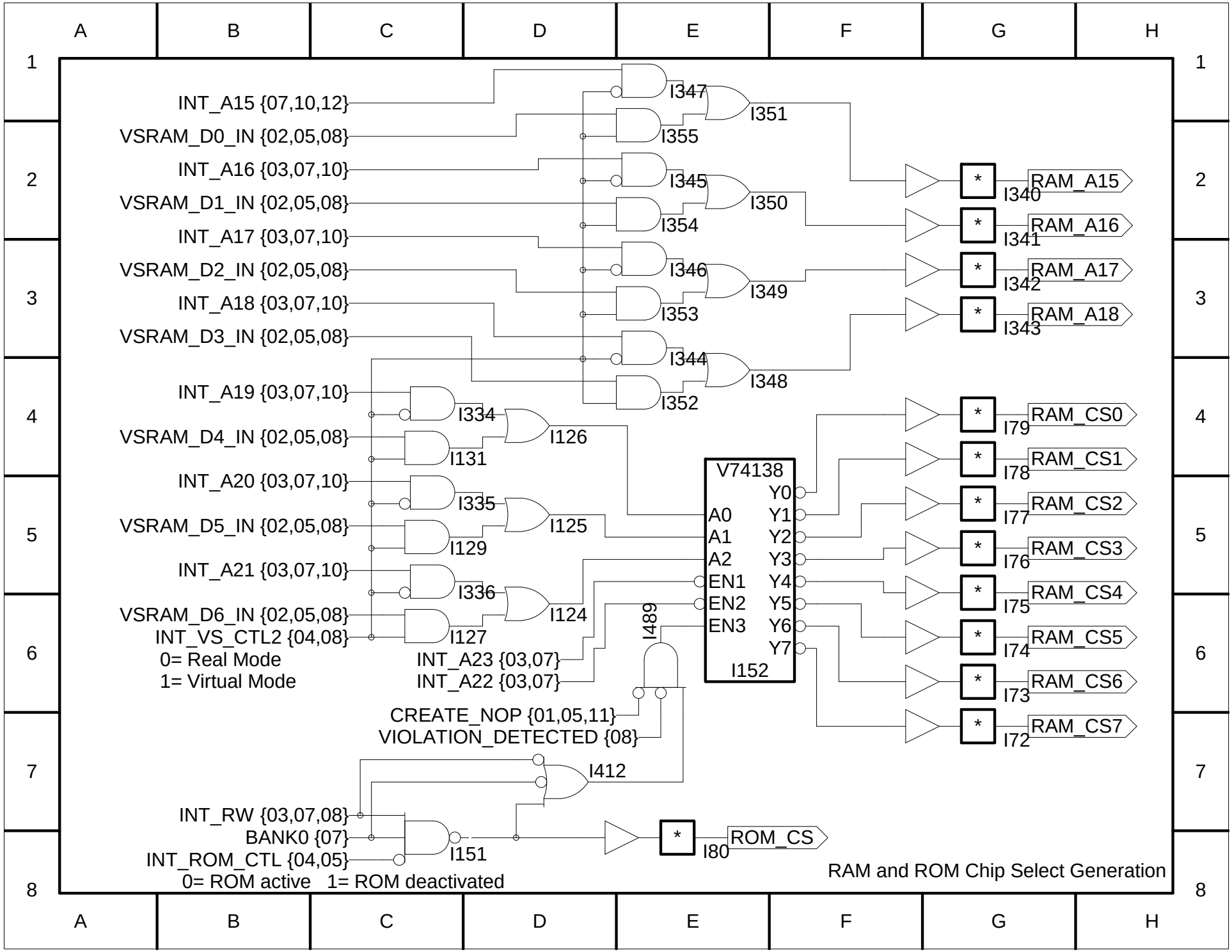

CPU_D0_IN {01,04,09,11}
VSRAM_D0_IN {05,06,08}
I32
VSRAM_D0
CPU_D1_IN {01,04,09,11}
VSRAM_D1_IN {05,06,08}
I31
VSRAM_D1
CPU_D2_IN {01,04,09,11}
VSRAM_D2_IN {05,06,08}
I30
VSRAM_D2
CPU_D3_IN {01,04,09,11}
VSRAM_D3_IN {05,06,08}
I29
VSRAM_D3
CPU_D4_IN {01,04,09,11}
VSRAM_D4_IN {05,06,08}
I28
VSRAM_D4
CPU_D5_IN {01,04,09,11}
VSRAM_D5_IN {05,06,08}
I27
VSRAM_D5
CPU_D6_IN {01,04,09,11}
VSRAM_D6_IN {05,06,08}
I26
VSRAM_D6
CPU_D7_IN {01,04,11}
VSRAM_D7_IN {05,08}
I25
VSRAM_D7
WR_VSRAM {07}
INT_PHI2 {01,08,11,12}
I413
INT_VSRAM_WR {03}
VSRAM Data I/O Lines

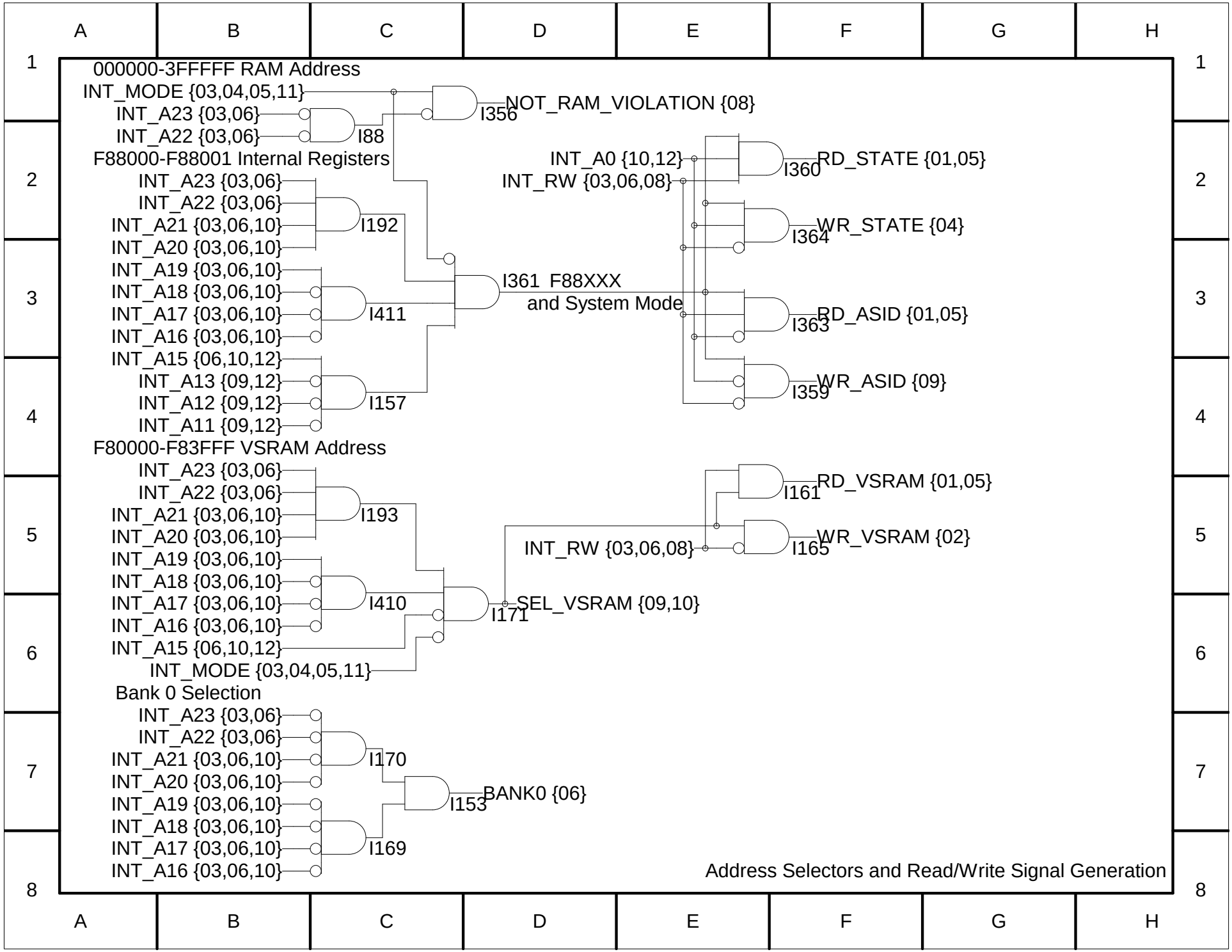


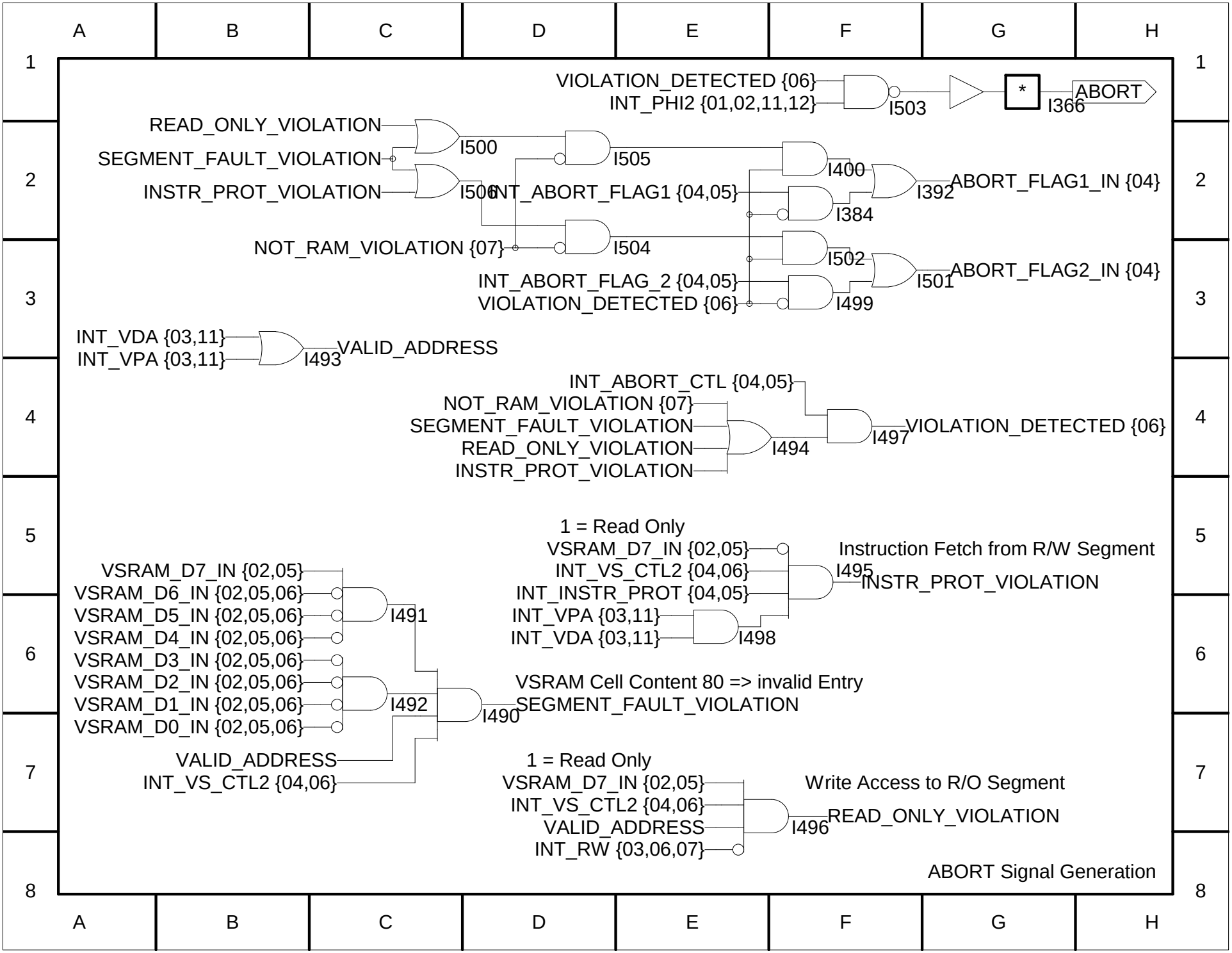
I/O-Lines and Emulation Mode Bank Address Generation

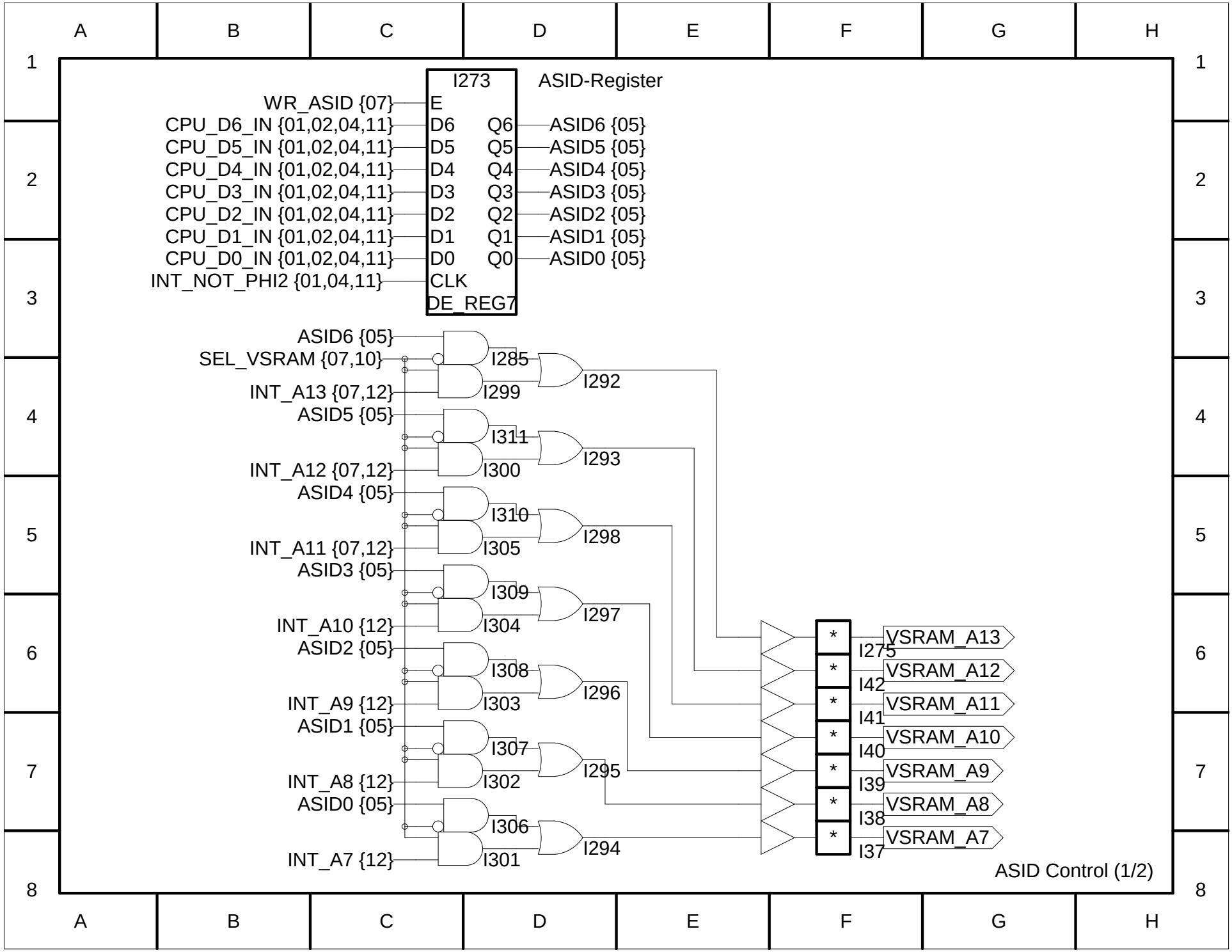

INT_NOT_PHI2 {01,09,11}
INT_VS_CTL {05}
CPU_D7_IN {01,02,11}
INT_ROM_CTL {05,06}
CPU_D6_IN {01,02,09,11}
INT_NMI_CTL {05,11}
CPU_D5_IN {01,02,09,11}
INT_ABORT_CTL {05,08}
CPU_D4_IN {01,02,09,11}
ABORT_FLAG2_IN {08}
CPU_D3_IN {01,02,09,11}
ABORT_FLAG1_IN {08}
CPU_D2_IN {01,02,09,11}
INT_INSTR_PROT {05,08}
CPU_D1_IN {01,02,09,11}
INT_MODE {03,05,07,11}
CPU_D0_IN {01,02,09,11}
WR_STATE {07}
INT_RES {03,11}
INT_VP {03,11}
INT_DMA_ACK {01,03,11}
I385
I406
I399
I380
I198
INT_VS_CTL2 {06,08}
I386
I401
I398
I378
I369
I390
I405
I397
I379
I370
I389
I404
I396
I376
I371
I388
I403
I395
I375
I367
I387
I402
I394
I374
I373
I485
I488
I487
I486
I372
I391
I407
I393
I377
I484
I382
I368
D Q
INT_VS_CTL {05}
VSTOR_CTL (Bit 7)
0= Real Mode
1= Virtual Mode
INT_ROM_CTL {05,06}
ROM_CTL (Bit 6)
0= ROM active
1= ROM deactivated
INT_NMI_CTL {05,11}
NMI_CTL (Bit 5)
0= NMI disabled
1= NMI enabled
INT_ABORT_CTL {05,08}
ABORT_CTL (Bit 4)
0= ABORT disabled
1= ABORT enabled
INT_ABORT_FLAG_2 {05,08}
ABORT Reason Code 2 (Bit 3)
INT_ABORT_FLAG1 {05,08}
ABORT Reason Code 1 (Bit 2)
INT_INSTR_PROT {05,08}
Instruction Protection (Bit 1)
0= Inactive
1= Active
INT_MODE {03,05,07,11}
MODE (Bit 0)
0= Supervisor Mode
1= User Mode
State Register

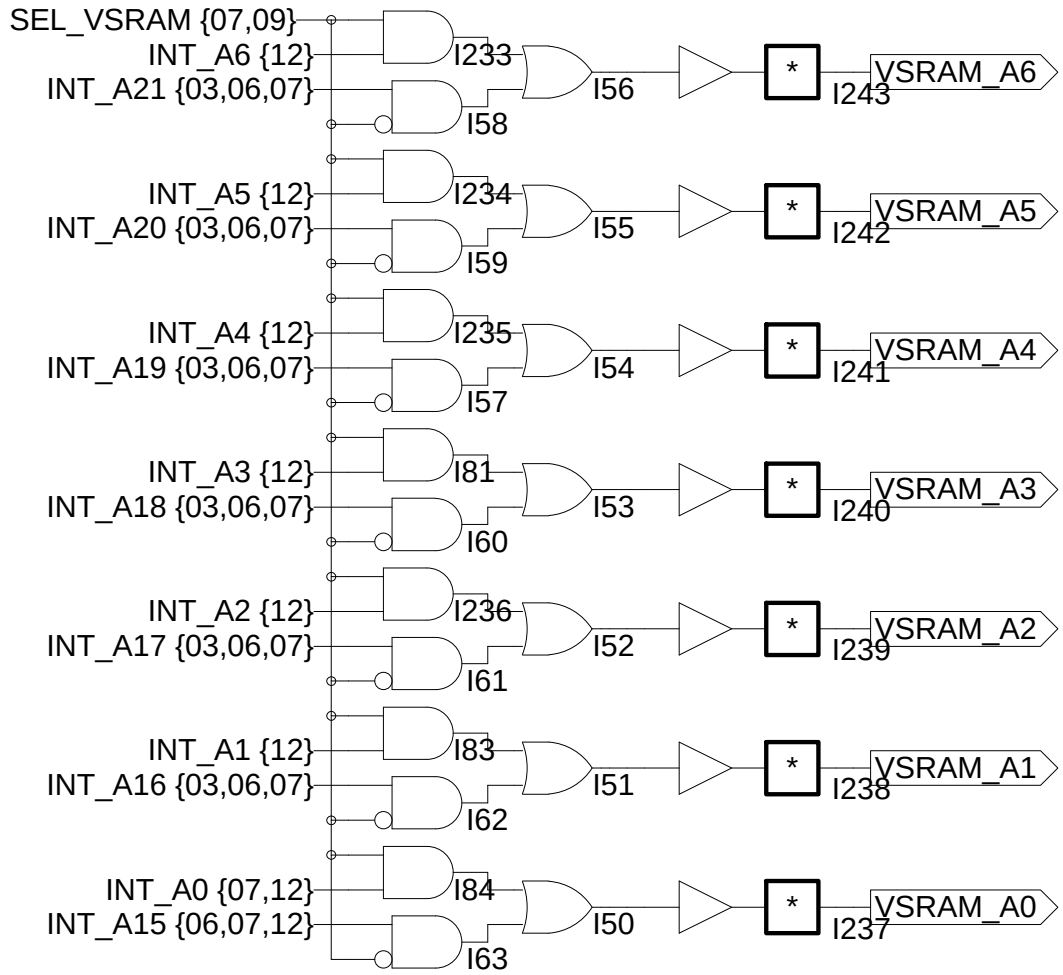

RD_VSRAM {01,07}
VSRAM_D7_IN {02,08}
VSRAM_D6_IN {02,06,08}
VSRAM_D5_IN {02,06,08}
VSRAM_D4_IN {02,06,08}
VSRAM_D3_IN {02,06,08}
VSRAM_D2_IN {02,06,08}
VSRAM_D1_IN {02,06,08}
VSRAM_D0_IN {02,06,08}
I112
I110
I197
I116
I115
I114
I113
I118
MMU_D7_OUT {01}
MMU_D6_OUT {01}
MMU_D5_OUT {01}
MMU_D4_OUT {01}
MMU_D3_OUT {01}
MMU_D2_OUT {01}
MMU_D1_OUT {01}
MMU_D0_OUT {01}
ASID6 {09}
ASID5 {09}
ASID4 {09}
ASID3 {09}
ASID2 {09}
ASID1 {09}
ASID0 {09}
RD_ASID {01,07}
I274
I223
I227
I108
I226
I225
I224
RD_ASID6 {01}
RD_ASID5 {01}
RD_ASID4 {01}
RD_ASID3 {01}
RD_ASID2 {01}
RD_ASID1 {01}
RD_ASID0 {01}
RD_STATE {01,07}
INT_VS_CTL {04}
INT_ROM_CTL {04,06}
INT_NMI_CTL {04,11}
INT_ABORT_CTL {04,08}
INT_ABORT_FLAG_2 {04,08}
INT_ABORT_FLAG1 {04,08}
INT_INSTR_PROT {04,08}
INT_MODE {03,04,07,11}
I284
I283
I282
I277
I281
I280
I279
I278
RD_STATE_D7 {01}
RD_STATE_D6 {01}
RD_STATE_D5 {01}
RD_STATE_D4 {01}
RD_STATE_D3 {01}
RD_STATE_D2 {01}
RD_STATE_D1 {01}
RD_STATE_D0 {01}
VCC
VCC
VCC
GND
VCC
GND
VCC
GND
CREATE_NOP {01,06,11}
I473
I474
I475
I476
I477
I478
I479
I480
NOP_OUT_D7 {01}
NOP_OUT_D6 {01}
NOP_OUT_D5 {01}
NOP_OUT_D4 {01}
NOP_OUT_D3 {01}
NOP_OUT_D2 {01}
NOP_OUT_D1 {01}
NOP_OUT_D0 {01}
Create NOP-Opcode (EA) for NMI-Signal
CPU Data Output Equates


INT_A15 {07,10,12}
VSRAM_D0_IN {02,05,08}
INT_A16 {03,07,10}
VSRAM_D1_IN {02,05,08}
INT_A17 {03,07,10}
VSRAM_D2_IN {02,05,08}
INT_A18 {03,07,10}
VSRAM_D3_IN {02,05,08}
INT_A19 {03,07,10}
VSRAM_D4_IN {02,05,08}
INT_A20 {03,07,10}
VSRAM_D5_IN {02,05,08}
INT_A21 {03,07,10}
VSRAM_D6_IN {02,05,08}
INT_VS_CTL2 {04,08}
0= Real Mode
1= Virtual Mode
INT_A23 {03,07}
INT_A22 {03,07}
CREATE_NOP {01,05,11}
VIOLATION_DETECTED {08}
INT_RW {03,07,08}
BANK0 {07}
INT_ROM_CTL {04,05}
0= ROM active 1= ROM deactivated
I347
I355
I351
I345
I354
I350
I346
I353
I349
I344
I352
I348
I334
I131
I126
I335
I129
I125
I336
I127
I124
I489
V74138
A0
A1
A2
EN1
EN2
EN3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
I152
I412
I151
I80
ROM_CS
I340
RAM_A15
I341
RAM_A16
I342
RAM_A17
I343
RAM_A18
I79
RAM_CS0
I78
RAM_CS1
I77
RAM_CS2
I76
RAM_CS3
I75
RAM_CS4
I74
RAM_CS5
I73
RAM_CS6
I72
RAM_CS7
RAM and ROM Chip Select Generation

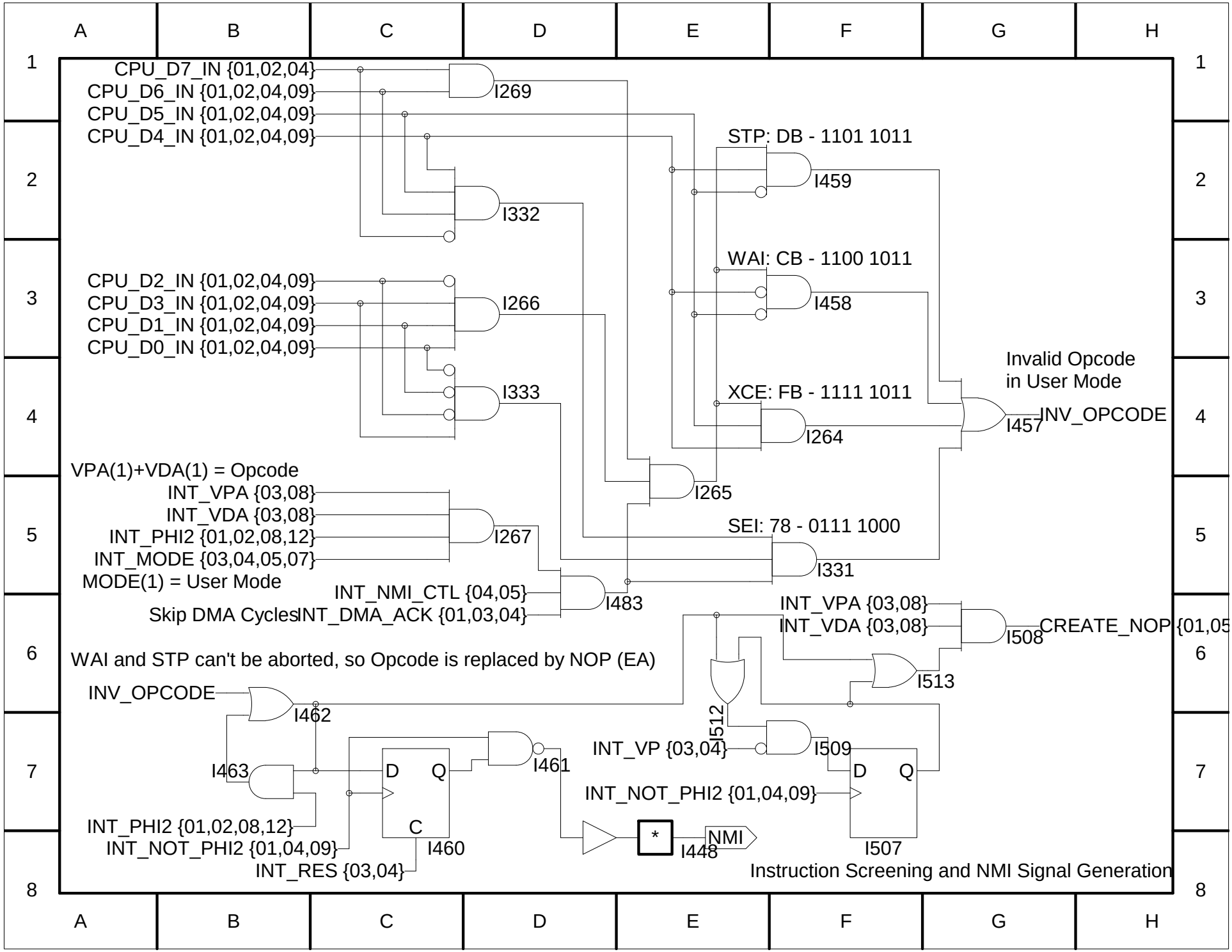

000000-3FFFFF RAM Address
INT_MODE {03,04,05,11}
INT_A23 {03,06}
INT_A22 {03,06}
I88
I356
NOT_RAM_VIOLATION {08}
F88000-F88001 Internal Registers
INT_A23 {03,06}
INT_A22 {03,06}
INT_A21 {03,06,10}
INT_A20 {03,06,10}
I192
INT_A19 {03,06,10}
INT_A18 {03,06,10}
INT_A17 {03,06,10}
INT_A16 {03,06,10}
I411
INT_A15 {06,10,12}
INT_A13 {09,12}
INT_A12 {09,12}
INT_A11 {09,12}
I157
I361 F88XXX
and System Mode
INT_A0 {10,12}
INT_RW {03,06,08}
I360
RD_STATE {01,05}
I364
WR_STATE {04}
I363
RD_ASID {01,05}
I359
WR_ASID {09}
F80000-F83FFF VSRAM Address
INT_A23 {03,06}
INT_A22 {03,06}
INT_A21 {03,06,10}
INT_A20 {03,06,10}
I193
INT_A19 {03,06,10}
INT_A18 {03,06,10}
INT_A17 {03,06,10}
INT_A16 {03,06,10}
I410
INT_A15 {06,10,12}
INT_MODE {03,04,05,11}
I171
SEL_VSRAM {09,10}
I161
RD_VSRAM {01,05}
INT_RW {03,06,08}
I165
WR_VSRAM {02}
Bank 0 Selection
INT_A23 {03,06}
INT_A22 {03,06}
INT_A21 {03,06,10}
INT_A20 {03,06,10}
I170
INT_A19 {03,06,10}
INT_A18 {03,06,10}
INT_A17 {03,06,10}
INT_A16 {03,06,10}
I169
I153
BANK0 {06}
Address Selectors and Read/Write Signal Generation

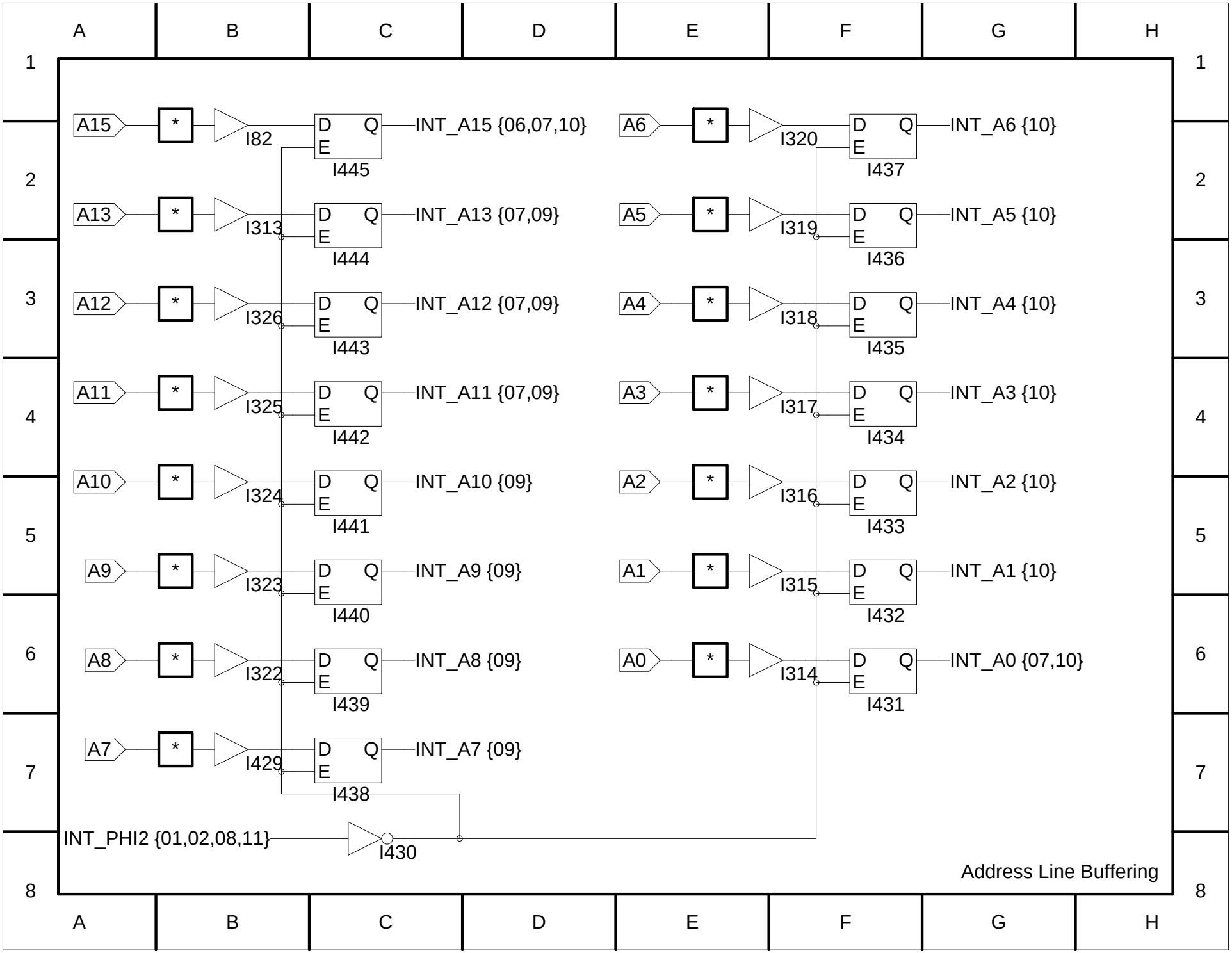

VIOLATION_DETECTED {06}
INT_PHI2 {01,02,11,12}
I503
*
I366
ABORT
READ_ONLY_VIOLATION
SEGMENT_FAULT_VIOLATION
INSTR_PROT_VIOLATION
I500
I505
I506
INT_ABORT_FLAG1 {04,05}
I400
I384
I392
ABORT_FLAG1_IN {04}
NOT_RAM_VIOLATION {07}
I504
I502
I501
ABORT_FLAG2_IN {04}
INT_ABORT_FLAG_2 {04,05}
VIOLATION_DETECTED {06}
I499
INT_VDA {03,11}
INT_VPA {03,11}
I493
VALID_ADDRESS
INT_ABORT_CTL {04,05}
NOT_RAM_VIOLATION {07}
SEGMENT_FAULT_VIOLATION
READ_ONLY_VIOLATION
INSTR_PROT_VIOLATION
I494
I497
VIOLATION_DETECTED {06}
1 = Read Only
VSRAM_D7_IN {02,05}
INT_VS_CTL2 {04,06}
INT_INSTR_PROT {04,05}
INT_VPA {03,11}
INT_VDA {03,11}
I495
I498
Instruction Fetch from R/W Segment
INSTR_PROT_VIOLATION
VSRAM_D7_IN {02,05}
VSRAM_D6_IN {02,05,06}
VSRAM_D5_IN {02,05,06}
VSRAM_D4_IN {02,05,06}
I491
VSRAM_D3_IN {02,05,06}
VSRAM_D2_IN {02,05,06}
VSRAM_D1_IN {02,05,06}
VSRAM_D0_IN {02,05,06}
I492
VALID_ADDRESS
INT_VS_CTL2 {04,06}
I490
VSRAM Cell Content 80 => invalid Entry
SEGMENT_FAULT_VIOLATION
1 = Read Only
VSRAM_D7_IN {02,05}
INT_VS_CTL2 {04,06}
VALID_ADDRESS
INT_RW {03,06,07}
I496
Write Access to R/O Segment
READ_ONLY_VIOLATION
ABORT Signal Generation


I273
ASID-Register
WR_ASID {07}
CPU_D6_IN {01,02,04,11}
CPU_D5_IN {01,02,04,11}
CPU_D4_IN {01,02,04,11}
CPU_D3_IN {01,02,04,11}
CPU_D2_IN {01,02,04,11}
CPU_D1_IN {01,02,04,11}
CPU_D0_IN {01,02,04,11}
INT_NOT_PHI2 {01,04,11}
E
D6
D5
D4
D3
D2
D1
D0
CLK
DE_REG7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
ASID6 {05}
ASID5 {05}
ASID4 {05}
ASID3 {05}
ASID2 {05}
ASID1 {05}
ASID0 {05}
ASID6 {05}
SEL_VSRAM {07,10}
INT_A13 {07,12}
ASID5 {05}
INT_A12 {07,12}
ASID4 {05}
INT_A11 {07,12}
ASID3 {05}
INT_A10 {12}
ASID2 {05}
INT_A9 {12}
ASID1 {05}
INT_A8 {12}
ASID0 {05}
INT_A7 {12}
I285
I299
I292
I311
I300
I293
I310
I305
I298
I309
I304
I297
I308
I303
I296
I307
I302
I295
I306
I301
I294
I275
I42
I41
I40
I39
I38
I37
VSRAM_A13
VSRAM_A12
VSRAM_A11
VSRAM_A10
VSRAM_A9
VSRAM_A8
VSRAM_A7
ASID Control (1/2)



ASID Control (2/2)


CPU_D7_IN {01,02,04}
CPU_D6_IN {01,02,04,09}
CPU_D5_IN {01,02,04,09}
CPU_D4_IN {01,02,04,09}
I269
I332
STP: DB - 1101 1011
I459
WAI: CB - 1100 1011
I458
CPU_D2_IN {01,02,04,09}
CPU_D3_IN {01,02,04,09}
CPU_D1_IN {01,02,04,09}
CPU_D0_IN {01,02,04,09}
I266
I333
XCE: FB - 1111 1011
I264
Invalid Opcode
in User Mode
I457
INV_OPCODE
VPA(1)+VDA(1) = Opcode
INT_VPA {03,08}
INT_VDA {03,08}
INT_PHI2 {01,02,08,12}
INT_MODE {03,04,05,07}
I267
I265
SEI: 78 - 0111 1000
I331
MODE(1) = User Mode
INT_NMI_CTL {04,05}
Skip DMA Cycles
INT_DMA_ACK {01,03,04}
I483
INT_VPA {03,08}
INT_VDA {03,08}
I508
CREATE_NOP {01,05
I513
WAI and STP can't be aborted, so Opcode is replaced by NOP (EA)
INV_OPCODE
I462
I512
INT_VP {03,04}
I509
I463
D
Q
I461
D
Q
INT_NOT_PHI2 {01,04,09}
INT_PHI2 {01,02,08,12}
C
INT_NOT_PHI2 {01,04,09}
I460
*
NMI
I448
I507
INT_RES {03,04}
Instruction Screening and NMI Signal Generation


A15
I82
I445
INT_A15 {06,07,10}
A13
I313
I444
INT_A13 {07,09}
A12
I326
I443
INT_A12 {07,09}
A11
I325
I442
INT_A11 {07,09}
A10
I324
I441
INT_A10 {09}
A9
I323
I440
INT_A9 {09}
A8
I322
I439
INT_A8 {09}
A7
I429
I438
INT_A7 {09}
INT_PHI2 {01,02,08,11}
I430
A6
I320
I437
INT_A6 {10}
A5
I319
I436
INT_A5 {10}
A4
I318
I435
INT_A4 {10}
A3
I317
I434
INT_A3 {10}
A2
I316
I433
INT_A2 {10}
A1
I315
I432
INT_A1 {10}
A0
I314
I431
INT_A0 {07,10}
Address Line Buffering